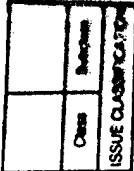


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**U.S. UTILITY** Patent Application

O.I.P.E. PATENT DATE  
*[Signature]*  
SCANNED TRA Q.A. 15

APPLICATION NO. 09/877027	CONT/PRIOR F	CLASS <u>257</u>	SUBCLASS 	ART UNIT <u>2811</u>	EXAMINER 
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Yasuhiko Tsukikawa

APPlicants

Configuration for generating a clock including a delay circuit and method thereof

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PTO-2040  
12/99

## **ISSUING CLASSIFICATION**

Continued on Issue Slip Inside File Jacket

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of the term of this patent has been disclaimed.				ISSUE BATCH NUMBER	

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